

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor(s): Jeong-Hun PARK, et al.  
Serial No.: 10/809,076 Examiner: Blum, David S  
Filing Date: March 24, 2004 Group Art Unit: 2813  
Confirmation No.: 7659  
Title: SEMICONDUCTOR PROCESS FOR REMOVING DEFECTS DUE TO  
EDGE CHIPS OF A SEMICONDUCTOR WAFER AND  
SEMICONDUCTOR DEVICE FABRICATED THEREBY

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Commissioner for Patents  
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Alexandria, VA 22313-1450

**APPLICANT'S COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR  
ALLOWANCE**

In the Examiner's Statement of Reasons for Allowance, the Examiner recited portions of the allowed independent claims and stated that the prior art failed to teach the recited portions. The applications note that it is a well known tenet of patent law that each allowed patent claim stands alone. Further, although the Examiner has indicated at least one reason for allowance, there are other reasons that claims are allowable. In other words, the Examiner has not recited all of the reasons for allowance, and there are reasons for allowability in addition to those given by the Examiner.

**Customer No. 20575**

Respectfully submitted,  
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